the priority setting means being associated with each of the peripheral devices for setting a selected priority level [in device status register means], and including device status register means in which the priority level is set;

[and (b)] the round robin register means having marker means for selecting the next [device] one of the peripheral devices to be serviced by the CPU, and also having advancing means for advancing the marker in the round robin register means to [the] a next [device] one of the peripheral devices at [the] a highest priority level in [said] the device status register means;

[characterised in that said] the peripheral devices [each] having respective priority setting means [which set] for setting the priority level for [that device] the respective one of the peripheral devices, depending on the urgency with which that device requires servicing.

2. A computer system according to claim 1, wherein the device status register means includes a separate device status register [is provided] for each of the priority [level] levels, [in the respective device status register means, and a corresponding] and wherein the round robin register [is provided in the round robin register means for each device status register] means includes a plurality of round robin registers, a corresponding one of the round robin registers being provided for each of the device status registers;[,] each round robin register containing a single bit; the computer system further including priority determining means for identifying [the] a highest priority level device status register with at least one bit set; [and means in] the marker advancing means also including means for advancing the marker in the round robin register means at [the] a highest active priority level.

3. (amended) A computer system according to [either previous] claim 1, wherein different ones of the peripheral devices have different sets of priority levels.

4. (amended) A computer system according to claim 3, wherein the peripheral devices are communication devices containing buffers and [the] wherein priority level signals are determined by the state of occupancy of their buffers.

5. (amended) A computer system according to claim 4, wherein some of the peripheral devices which receive data at a higher rate[, or have a smaller buffer,] may switch to a higher priority level at lower levels of buffer occupancy [(or emptiness in the case of an output device)] than others.

6. (amended) A computer system according to claim [4 or] 5, wherein when [a device] one of the peripheral devices produces a signal of the appropriate priority level, it may produce signals of lower priority level.

7. (amended) A computer system according to [any preceding] claim 6, wherein lock-out of the devices is prevented by raising the device priority as servicing becomes more urgent, and once all devices at the highest active priority level are fully serviced, the priority level is dropped to a lower level, and servicing of devices at that level recommences; servicing of devices at the new lower level recommencing at a point where it was left off when a higher priority level up became active.

8. (amended) A computer system according to [any preceding] claim 6, wherein the system includes means for allocating more system resources to the CPU in response to detection that one or more devices are becoming in need of urgent servicing.

Please add the following claims.

9. (new) A computer system according to claim 2, wherein different ones of the peripheral devices have different sets of priority levels.

10. (new) A computer system according to claim 9, wherein the peripheral devices are communication devices containing buffers and wherein priority level signals are determined by the state of occupancy of their buffers.

11. (new) A computer system according to claim 10, wherein some of the peripheral devices which receive data at a higher rate may switch to a higher priority level at lower levels of buffer occupancy than others.

12. (new) A computer system according to claim 11, wherein when one of the peripheral devices produces a signal of the appropriate priority level, it may produce signals of lower priority level.

13. (new) A computer system according to claim 1, wherein the priority setting means is operable to raise priority of the respective peripheral device, as servicing becomes more urgent, for preventing lockout of the peripheral device; and wherein the priority setting means is operable to drop the priority level to a lower level once all of the peripheral devices at the highest active priority level are fully serviced, whereby servicing of the peripheral devices at that level recommences; servicing of the peripheral devices at a new lower level recommencing at a point where it was left off when a higher priority level became active.

14. (new) A computer system according to claim 1, further including means for allocating more system resources to the CPU in response to detection of a state wherein one or more of the peripheral devices are becoming in need of urgent servicing.

15. (new) A computer system according to claim 4, wherein some of the peripheral devices which have a smaller buffer for receiving data may switch to a higher priority level at lower levels of buffer occupancy than others.

16. (new) A computer system according to claim 4, wherein some of the peripheral devices which transmit data at a higher rate may switch to a higher priority level at higher levels of buffer occupancy than others.

17. (new) A computer system according to claim 4, wherein some of the peripheral devices which have a smaller buffer for transmitting data may switch to a higher priority level at higher levels of buffer occupancy than others.

18. (new) A computer system according to claim 10, wherein some of the peripheral devices which have a smaller buffer for receiving data may switch to a higher priority level at lower levels of buffer occupancy than others.